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Fellers, Snider, Blankenship, Bailey & Tippens, P.C. Suite 1700 100 North Broadway Oklahoma City, OK 73102-8820			EXAMINER	
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte SUNDEEP CHAUHAN

Appeal 2009-003915 Application 10/625,386 Technology Center 2800

Decided: August 11, 2009

Before JOSEPH F. RUGGIERO, ROBERT E. NAPPI, and CARL W. WHITEHEAD JR., *Administrative Patent Judges*.

NAPPI, Administrative Patent Judge.

DECISION ON APPEAL

Application 10/625,386

This is a decision on appeal under 35 U.S.C. § 6(b) of the rejection of claims 1 through 3, 7 through 12, 16 through 22, 25, and 26.

We affirm-in-part.

INVENTION

The invention is directed to an apparatus to detect the difference between an input and a reference signal in a digital phase locked loop. See page 5 of Appellant's Specification. Claims 1 and 10 are reproduced below:

- 1. An apparatus comprising a phase/frequency comparator circuit that is configured to generate a phase error responsive to a transition location signal.
- 10. A phase locked loop comprising:
- a controllable oscillator; and
- a phase/frequency comparator coupled to the controllable oscillator such that an output of the controllable oscillator is connected in a feedback loop to an input of the phase/frequency comparator and an output of the phase/frequency comparator is connected through a forward path to a control input of the controlled oscillator,

wherein the phase/frequency comparator includes:

a phase detecting stage; encoding circuitry coupled to the phase detecting stage; and an accumulator coupled to the encoding circuitry.

REFERENCES

Brachmann	US 6,351,154 B2	Feb. 26, 2002
Staszewski	US 6,429,693 B1	Aug. 6, 2002

REJECTIONS AT ISSUE

The Examiner has rejected claims 1 through 3, 7, 10-12, 16, 17, 20-22, 25, and 26 under 35 U.S.C. § 102(e) as being anticipated by Staszewski. The Examiner's rejection is on pages 3 through 5 of the Answer. ¹

The Examiner has rejected claims 8 and 18 under 35 U.S.C. § 103(a) as being unpatentable over Staszewski in view of Brachmann. The Examiner's rejection is on page 6 of the Answer.

The Examiner has rejected claims 9 and 19 under 35 U.S.C. § 103(a) as being unpatentable over Staszewski. The Examiner's rejection is on page 6 of the Answer.

ISSUES

Rejection of claims 1 through 3, 7, 20 through 22, 25, and 26 under 35 U.S.C. § 102(e).

Appellant argues on pages 5 through 13 of the Brief² that the Examiner's rejection of claims 1 through 3, 7, 20-22, 25, and 26 under 35 U.S.C. § 102(e) is in error. Appellant argues that the phrase "transition location signal" of claim 1³, should be interpreted as "a signal that indicates a translation location." Brief 6. Appellant argues that, contrary to the Examiner's finding, the snapshot signal 604 of Staszewski does not meet the claimed transition location signal. Appellant argues that the snapshot signal represents a timing difference and not a location signal and, further, that

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¹ Throughout the opinion we refer to the Answer mailed February 25, 2008.

² Throughout the opinion we refer to the Brief dated November 21, 2007 and Reply Brief dated April 25, 2008.

³ Appellant's arguments group claims 1 through 3, 7, 20 through 22, 25, and 26 together, we select claim 1 as representative of the group.

Appeal 2009-003915 Application 10/625,386

there are different locations where the value of signal 604 will be the same. Brief 10 through 12.

Thus, Appellant's contentions directed to the rejection of claims 1 through 3, 7, 20-22, 25, and 26 present us with the issue:

Has Appellant shown that the Examiner erred in finding that the snapshot signal 604 of Staszewski meets the claimed transition location signal?

Rejection of claims 10 through 12, 16, and 17 under 35 U.S.C. § 102(e).

Appellant argues on page 13 through 15 of the Brief that the Examiner's rejection of claims 10 through 12, 16, and 17 under 35 U.S.C. § 102(e) is in error. Appellant argues that independent claim 10 recites "encoding circuitry coupled to the phase detecting stage" and that the Examiner has not shown that Staszewski teaches this feature. Brief 13.

Thus, Appellant's arguments with respect to claims 10 through 12, 16, and 17 present us with the issue, has Appellant shown that the Examiner erred in finding that Staszewski teaches an encoder as recited in claim 10?

PRINCIPLES OF LAW

Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. *RCA Corp. v. Appl. Dig. Data Sys., Inc.*, 730 F.2d 1440, 1444 (Fed. Cir. 1984); *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554 (Fed. Cir. 1983).

FINDINGS OF FACT

Staszewski

- 1. Staszewski teaches digital phase detector. Abstract.
- 2. The system calculates a composite phase error using a fractional-division-ratio corrected value ∈(k). Col 7, ll. 43-49.
- 3. The value \in (k) is calculated using the measured values Δt_r and Δt_f . Col. 7, Il. 18-30.
- 4. The value Δt_r represents the time between the rising edge of signal CKV and the rising edge FREF. Similarly, the value Δt_f represents the time between the falling edge of signal CKV and the rising edge of FREF. The time values are referred to as position with respect to sampling edge of FREF. See Figures 3 and 4, col. 6, ll. 44-51.
- 5. Figure 6 depicts a different embodiment of sampling to determine the values Δt_r and Δt_f . We note in Figure 6 the values are referred to as TDC_RISE and TDC_FALL. In Figure 6, the snapshot item 604 represents a series of delays in signal CKV relative to the rising edge of the FREF. Col. 8, 11. 39-45.

ANALYSIS

Rejection of claims 1 through 3, 7, 20 through 22, 25, and 26 under 35 U.S.C. § 102(e).

Appellant has not persuaded us that the Examiner erred in finding that the snapshot signal 604 of Staszewski meets the claimed transition location signal. Claim 1 recites "generating a phase error in response to a translation location signal." Appellant asserts that "the phrase *transition location signal*

ordinarily means a <u>signal</u> that indicates a <u>transition location</u>." Brief 6. We accept the Appellant's proffered definition of the term, however we note that based upon the description in Appellant's Specification the position is a position in time (over one cycle of a reference clock) from either a rising or falling edge. Specification 7:1-10. Thus, interpreted in light of the Appellant's Specification, the limitation of the "transition location signal" is a signal that represents the position in time and within one cycle of the reference clock of a transition.

The Examiner has found that the Staszewski's signal, item 604 (before being converted to TDC_RISE, and TDC_FALL) meets the claimed translation location signal. Answer 3. Appellant argues on page 9 of the Brief, and page 3 of the Reply Brief, that Staszewski's signal, item 604, is a timing signal and not a position signal. This argument has not persuaded us of error. Initially, we note that as discussed above the "location signal" is a location in time, thus the claimed signal is also a timing signal. Further, Staszewski teaches that the signal represents a position in time between the rising edge of FREF and the rising edge of CKV. Facts 4 and 5. Thus, we find that Staszewski's signal item 604 is a "location signal" as interpreted in light of the Appellant's Specification.

Appellant also argues that the snapshot signal 604 is not a location signal as there are "different locations that the FREF transition 602 could occur and yet be associated with the same snapshot signal 604." Brief 10. Appellant proffers a hypothetical example to support this argument and relies upon there being two locations (in time) in the traces of Staszewski's figure 6 where the value of signal 604 would be the same, where one of the locations is prior to the rising edge of signal CKV. Brief 10, Reply Brief 4.

This argument is not persuasive of error. The signal 604 of Staszewski depicts the number of delays between the rising edge of signal CKV and the rising edge of the signal FREF (i.e. this is a measure of the delay within one cycle). Facts 4 and 5. We do not find that the evidence supports the Appellant's example because the hypothetical location for signal 604 is prior to the rising edge of signal CKV, not between rising edges of the two signals. As such, Appellant's arguments have not persuaded us that the Examiner erred in finding that the snapshot signal 604 of Staszewski meets the claimed transition location signal. As this is the only issue directed to the Examiner's rejection of claims 1 through 3, 7, 20 through 22, 25, and 26 under 35 U.S.C. § 102(e), we sustain the Examiner's rejection.

Rejections of claims 8 and 9 under 35 U.S.C. § 103(a).

Appellant's augments do not address the rejections of claims 8 and 9 under 35 U.S.C. § 103(a). These claims depend upon claim 1 and the Examiner's rejections of these claims rely upon the teachings of Staszewski to teach the limitations of claim 1. Accordingly, we sustain the Examiner's rejections of claims 8 and 9 for the reasons discussed with respect to the Examiner's rejection of claim 1 under 35 U.S.C. § 102(e).

Rejection of claims 10 through 12, 16, and 17 under 35 U.S.C. § 102(e).

Appellant's arguments have persuaded us that the Examiner erred in finding that Staszewski teaches an encoder as recited in claim 10. The Examiner has interpreted the claim term encoder as a device to "convert an input digital signal into its equivalent binary code." Answer 7 and 8. The

Examiner finds that Staszewski's circuit "NORM" of Figure 2 meets the claimed encoder and cites to Staszewski column 5, line 64- column 6, line 43, to support this assertion. Answer 8. We disagree with the Examiner's finding. We note that the section of Staszewski cited by the Examiner does not identify the circuit "NORM" by name. It appears from our review of Staszewski that the circuit NORM, which receives inputs Δt_r , and Δt_f and outputs either \in (k) or Φ_F , is performing the calculations set forth in equations 10 and 11 of Staszewski (see column 7). We do not find that these equations represent the conversion of an input digital signal into its equivalent binary code. Thus, we do not find that the Examiner has shown that Staszewski teaches all of the limitations of independent claim 10. Claims 11, 12, 16, and 17 all depend upon claim 10 and as such include the same limitation. Accordingly, we will not sustain the Examiner's rejection of claims 10 through 12, 16, and 17.

Rejections of claims 18 and 19 under 35 U.S.C. § 103(a).

Claims 18 and 19 depend upon claim 10 and the Examiner's rejections of these claims rely upon the teachings of Staszewski to teach the limitations of claim 10. Accordingly, we will not sustain the Examiner's rejections of claims 18 and 19 for the reasons discussed with respect to the Examiner's rejection of claim 10 under 35 U.S.C. § 102(e).

CONCLUSION

Appellant has not persuaded us of error in the Examiner's rejections of claims 1 through 3, 7 through 9, 20 through 22, 25, and 26. However, Appellant's arguments have persuaded us of error in the Examiner's rejections of claims 10 through 12, 16, and 17, 18 and 19.

ORDER

The decision of the Examiner to reject claims 1 through 3, 7 through 12, 16 through 22, 25, and 26 is affirmed-in-part.

Appeal 2009-003915 Application 10/625,386

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

ELD

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